

WHAT IS CLAIMED IS:

1. A semiconductor device having a non-volatile memory transistor, comprising:

a capacitor element and another capacitor element,

5 the non-volatile memory transistor, the capacitor element and the another capacitor element being formed in one semiconductor substrate,

the capacitor element including a lower electrode, a dielectric film and an upper electrode,

10 the another capacitor element having another lower electrode, another dielectric film and another upper electrode, and

the another dielectric film having a film thickness that is different from a film thickness of the dielectric film.

2. A semiconductor device having a non-volatile memory transistor, comprising:

a capacitor element and another capacitor element,

the non-volatile memory transistor, the capacitor element and the another capacitor element being formed in one semiconductor substrate,

20 the capacitor element including a lower electrode, a dielectric film having a plurality of films as components and an upper electrode,

the another capacitor element having another lower electrode, another dielectric film having a plurality of films as components and another upper electrode, and

25 the components of the another dielectric film being different from the components of the dielectric films.

3. A semiconductor device according to claim 1 or claim 2, wherein the dielectric film and the another dielectric film include an ONO film.

4. A semiconductor device according to claim 3, wherein

the dielectric film has a structure including a thermal oxidation film, a nitride film and an oxide film successively laid in a direction from the lower electrode toward the upper electrode, and

5 the another dielectric film has a structure including a first thermal oxide film, a CVD oxide film, a second thermal oxide film, a nitride film and an oxide film successively laid in a direction from the another lower electrode toward the another upper electrode.

10 5. A semiconductor device according to claim 3, wherein

the dielectric film has a structure including only a thermal oxidation film, a nitride film and an oxide film successively laid in a direction from the lower electrode toward the upper electrode, and

15 the another dielectric film has a structure including only a first thermal oxide film, a CVD oxide film, a second thermal oxide film, a nitride film and an oxide film successively laid in a direction from the another lower electrode toward the another upper electrode.

20 6. A semiconductor device according to claim 4 or claim 5, wherein the thermal oxide film of the dielectric film and the second thermal oxide film of the another dielectric film are films that are formed in the same step,

the nitride film of the dielectric film and the nitride film of the another dielectric film are films that are formed in the same step, and

25 the oxide film of the dielectric film and the oxide film of the another dielectric film are films that are formed in the same step.

7. A semiconductor device according to claim 4 or claim 5, wherein the CVD oxide film of the another dielectric film includes a high-temperature CVD oxide film.

5 8. A semiconductor device according to claim 4 or claim 5, wherein each of the oxide film of the dielectric film and the oxide film of the another dielectric film includes a thermal oxide film.

9. A semiconductor device according to claim 8, wherein
10 the thermal oxide film of the dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 –200 angstrom,

the nitride film of the dielectric film has a thickness of 50 – 500 angstrom,

15 the oxide film of the dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom,

the first thermal oxide film of the another dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom,

20 the CVD oxide film of the another dielectric film has a thickness of 100 – 200 angstrom,

the second thermal oxide film of the another dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 – 200 angstrom,

25 the nitride film of the another dielectric film has a thickness of 50 – 500 angstrom, and

the oxide film of the another dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 –80 angstrom.

5 10. A semiconductor device according to claim 4 or claim 5, wherein each of the oxide film of the dielectric film and the oxide film of the another dielectric film includes a CVD oxide film.

10 11. A semiconductor device according to claim 10, wherein the thermal oxide film of the dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 –200 angstrom,

the nitride film of the dielectric film has a thickness of 50 – 500 angstrom,

15 the oxide film of the dielectric film has a thickness of 100 – 200 angstrom.

the first thermal oxide film of the another dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom,

20 the CVD oxide film of the another dielectric film has a thickness of 100 – 200 angstrom,

the second thermal oxide film of the another dielectric film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 30 – 200 angstrom,

25 the nitride film of the another dielectric film has a thickness of 50 – 500 angstrom, and

the oxide film of the another dielectric film has a thickness of 100 – 200 angstrom.

12. A semiconductor device according to claim 1 or claim 2, wherein the upper electrode and the another upper electrode are electrodes formed from polysilicon.

5 13. A semiconductor device according to claim 1 or claim 2, wherein the upper electrode and the another upper electrode are electrodes formed from polycide.

10 14. A semiconductor device according to claim 1 or claim 2, wherein the upper electrode and the another upper electrode are electrodes formed from metal.

15 15. A semiconductor device according to claim 1 or claim 2, wherein the upper electrode and the another upper electrode are electrodes formed from salicide.

20 16. A semiconductor device according to claim 1 or claim 2, wherein the lower electrode and the another lower electrode are films that are formed in the same step, and the upper electrode and the another upper electrode are films that are formed in the same step.

 17. A semiconductor device according to claim 4 or claim 5, wherein the non-volatile memory transistor includes
 a floating gate,
25 a control gate, and
 an intermediate insulation film located between the floating gate and the control gate, wherein

the intermediate insulation film has a structure having a first thermal oxide film, a CVD oxide film, a second thermal oxide film and an oxide film that are successively disposed in a direction from the floating gate toward the control gate.

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18. A semiconductor device according to claim 17, wherein

the first thermal oxide film of the intermediate insulation film and the first thermal oxide film of the another dielectric film are films that are formed in the same step,

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the CVD oxide film of the intermediate insulation film and the CVD oxide film of the another dielectric film are films that are formed in the same step,

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the second thermal oxide film of the intermediate insulation film, the thermal oxide film of the dielectric film and the second thermal oxide film of the another dielectric film are films that are formed in the same step, and

the oxide film of the intermediate insulation film, the oxide film of the dielectric film and the oxide film of the another dielectric film are films that are formed in the same step.

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19. A semiconductor device according to claim 17, wherein the intermediate insulation film includes a nitride film, wherein

the nitride film of the intermediate insulation film is located below a sidewall of the floating gate and between the second thermal oxide film of the intermediate insulation film and the oxide film of the intermediate insulation film.

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20. A semiconductor device according to claim 19, wherein the nitride film of the intermediate insulation film, the nitride film of the dielectric film

and the nitride film of the another dielectric film are films that are formed in the same step.

21. A semiconductor device according to claim 17, wherein the CVD
5 oxide film of the intermediate insulation film includes a high-temperature thermal CVD oxide film.

22. A semiconductor device according to any one of claim 17 through
claim 21, wherein the oxide film of the intermediate insulation film includes at
10 least one of a thermal oxide film and a CVD oxide film.

23. A semiconductor device according to claim 17, wherein the control
gate, the upper electrode and the another upper electrode are electrodes that
are formed from polysilicon.
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24. A semiconductor device according to claim 17, wherein the control
gate, the upper electrode and the another upper electrode are electrodes that
are formed from polycide.

25. A semiconductor device according to claim 17, wherein the control
gate, the upper electrode and the another upper electrode are electrodes that
are formed from metal.
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26. A semiconductor device according to claim 17, wherein the control
gate, the upper electrode and the another upper electrode are electrodes that
are formed from salicide.
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27. A semiconductor device according to claim 17, wherein the floating gate, the lower electrode and the another lower electrode are films that are formed in the same step, and

the control gate, the upper electrode and the another upper electrode
5 are films that are formed in the same step.

28. A semiconductor device according to claim 1 or claim 2, wherein an area of the upper electrode that faces a surface of the dielectric film is the same as an area of the another upper electrode that faces a surface of the
10 another dielectric film.

29. A semiconductor device according to claim 1 or claim 2, wherein an area of the upper electrode that faces a surface of the dielectric film is different from an area of the another upper electrode that faces a surface of the
15 another dielectric film.

30. A semiconductor device according to claim 1 or claim 2, wherein the another lower electrode has an impurity concentration different from an impurity concentration of the lower electrode.
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31. A semiconductor device according to claim 1 or claim 2, wherein the dielectric film has a film thickness of 180 – 900 angstrom, and the another dielectric film has a film thickness of 340 – 1180 angstrom.

32. A semiconductor device according to claim 1 or claim 2, wherein
25 the capacitor element has a capacitor value that is different from a capacitor value of the another capacitor element.

33. A semiconductor device according to claim 1 or claim 2, wherein each of the capacitor element and the another capacitor element is a component of an analogue circuit.

5 34. A semiconductor device according to claim 1 or claim 2, wherein the non-volatile memory transistor includes a split-gate type non-volatile memory transistor.

10 35. A method for manufacturing a semiconductor device having a structure that includes a non-volatile memory transistor, a capacitor element and another capacitor element formed in one semiconductor substrate, wherein the non-volatile memory transistor includes a floating gate, an intermediate insulation film and a control gate,

15 the capacitor element includes a lower electrode, a dielectric film and an upper electrode, and

 the another capacitor element has another lower electrode, another dielectric film and another upper electrode, the method comprising the steps of:

- (a) forming the floating gate, the lower electrode and the another lower electrode on the semiconductor substrate;
- 20 (b) forming a first oxide film on the floating gate, the lower electrode and the another lower electrode;
- (c) forming a second oxide film on the first oxide film;
- (d) patterning the first oxide film and the second oxide film to thereby leave the first oxide film and the second oxide film that
- 25 become components of the intermediate insulation film on sidewalls on the floating gate, to remove the first oxide film and the second oxide film on the lower electrode, and to leave the first

oxide film and the second oxide film that become components of the another dielectric film on the another lower electrode;

- 5 (e) forming a third oxide film that becomes a component of the intermediate insulation film, a component of the dielectric film and a component of the another dielectric film on the second oxide film on the sidewall of the floating gate, the lower electrode and the second oxide film on the another lower electrode, respectively,
- 10 (f) forming a nitride film that becomes a component of the dielectric film and a component of the another dielectric film on the third oxide film on the lower electrode and the third oxide film on the another lower electrode, respectively,
- 15 (g) forming a fourth oxide film that becomes a component of the intermediate insulation film, a component of the dielectric film and a component of the another dielectric film on the third oxide film on the sidewall of the floating gate, the nitride film on the lower electrode and the nitride film on the another lower electrode, respectively, and
- 20 (h) forming, after the step (g), the control gate, the upper electrode and the another upper electrode on the semiconductor substrate.

36. A method for manufacturing a semiconductor device according to claim 35, wherein the step (a) includes the step of introducing an impurity in the lower electrode to make the lower electrode to have a first impurity concentration, and the step of introducing an impurity in the another lower electrode to make the another lower electrode to have a second impurity concentration that is different from the first impurity concentration.

37. A method for manufacturing a semiconductor device according to claim 35, wherein the first oxide film is formed by thermal oxidation.

38. A method for manufacturing a semiconductor device according to
5 claim 35, wherein the second oxide film is formed by CVD.

39. A method for manufacturing a semiconductor device according to claim 38, wherein the CVD includes a high-temperature CVD.

10 40. A method for manufacturing a semiconductor device according to claim 35, wherein the third oxide film is formed by thermal oxidation.

41. A method for manufacturing a semiconductor device according to claim 35, wherein the nitride film is formed by CVD.

15 42. A method for manufacturing a semiconductor device according to claim 35, wherein the fourth oxide film is formed by thermal oxidation.

20 43. A method for manufacturing a semiconductor device according to claim 35, wherein the fourth oxide film is formed by CVD.

44. A method for manufacturing a semiconductor device according to claim 35, wherein the step (f) includes the steps of:

forming a nitride film on the third oxide film;

25 forming a mask film on the nitride film on the third oxide film over the lower electrode and on the nitride film on the third oxide film over the another lower electrode;

selectively removing the nitride film by anisotropic etching, using the mask film as a mask to leave the nitride film that becomes a component of the intermediate insulation film, a component of the dielectric film and a component of the another dielectric film on the third oxide film on a sidewall lower section of the floating gate, on the third oxide film on the lower electrode and on the third oxide film on the another lower electrode, respectively.

45. A method for manufacturing a semiconductor device according to claim 35, wherein the step (a) includes the step of forming a selective oxide film on the floating gate.

46. A method for manufacturing a semiconductor device according to claim 45, wherein the step of forming the selective oxide film includes the steps of:

forming a conductive film on the semiconductor substrate; and forming the selective oxide film on the conductive film that becomes the floating gate.

47. A method for manufacturing a semiconductor device according to claim 46, wherein the floating gate is patterned, using the selective oxide film as a mask.

48. A method for manufacturing a semiconductor device according to any one of claim 35 through claim 44, wherein the step (a) includes the steps of: forming a conductive film on the semiconductor substrate; and patterning the conductive film to form the floating gate, the lower electrode and the another lower electrode at the same time.

49. A method for manufacturing a semiconductor device according to claim 35, wherein the step (h) includes the steps of:

forming another conductive film on the semiconductor substrate; and
patterning the another conductive film to form the control gate, the
5 upper electrode and the another upper electrode at the same time.

50. A method for manufacturing a semiconductor device according to claim 35, wherein the non-volatile memory transistor includes a split-gate type non-volatile memory transistor.

51. A semiconductor device having a non-volatile memory transistor, comprising:

a capacitor element,

wherein the non-volatile memory transistor and the capacitor element
15 are formed in one semiconductor substrate,

the capacitor element includes a lower electrode, a dielectric film and an upper electrode, and

the dielectric film has a structure that includes a first oxide film, a second oxide film, a nitride film and a third oxide film successively laid in a
20 direction from the lower electrode toward the upper electrode.

52. A semiconductor device having a non-volatile memory transistor, comprising:

a capacitor element,

wherein the non-volatile memory transistor and the capacitor element
25 are formed in one semiconductor substrate,

the capacitor element includes a lower electrode, a dielectric film and an upper electrode,

the dielectric film having a structure that includes only a first oxide film, a second oxide film, a nitride film and a third oxide film successively laid in a direction from the lower electrode toward the upper electrode.

5 53. A semiconductor device according to claim 51 or claim 52, wherein the first oxide film includes a thermal oxide film, the second oxide film includes a CVD oxide film and the third oxide film includes a thermal oxide film.

10 54. A semiconductor device according to claim 53, wherein the second oxide film includes a high-temperature CVD oxide film.

15 55. A semiconductor device according to claim 53, wherein the first oxide film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom, the second oxide film has a thickness of 100 – 200 angstrom, the nitride film has a thickness of 50 – 500 angstrom, and the third oxide film has a thickness grown by a method that grows a thermal oxide film on silicon to a thickness of 60 – 80 angstrom.

20 56. A semiconductor device according to claim 51 or claim 52, wherein the non-volatile memory transistor includes a floating gate, a control gate, and an intermediate insulation film located between the floating gate and the control gate,

25 the intermediate insulation film having a structure that includes a first oxide film, a second oxide film and a third oxide film successively provided in a direction from the floating gate toward the control gate.

57. A semiconductor device according to claim 56, wherein

the first oxide film of the intermediate insulation film includes a thermal oxide film,

the second oxide film of the intermediate insulation film includes a CVD oxide film, and

5 the third oxide film of the intermediate insulation film includes a thermal oxide film.

58. A semiconductor device according to claim 57, wherein the second oxide film of the intermediate insulation film includes a high-temperature CVD
10 oxide film.

59. A semiconductor device according to claim 56, wherein the first oxide film of the intermediate insulation film and the first oxide film of the dielectric film are formed in the same step,

15 the second oxide film of the intermediate insulation film and the second oxide film of the dielectric film are formed in the same step, and

the third oxide film of the intermediate insulation film and the third oxide film of the dielectric film are formed in the same step.

20 60. A semiconductor device according to claim 56, wherein the intermediate insulation film includes a nitride film, wherein the nitride film of the intermediate insulation film is located below the sidewall of the floating gate and between the second oxide film of the intermediate insulation film and the third oxide film of the intermediate insulation film.

25 61. A semiconductor device according to claim 60, wherein the nitride film of the intermediate insulation film and the nitride film of the dielectric film are films that are formed in the same step.

62. A semiconductor device according to claim 56, wherein the control gate and the upper electrode are electrodes that are formed from polysilicon.

5 63. A semiconductor device according to claim 56, wherein the control gate and the upper electrode are electrodes that are formed from polycide.

64. A semiconductor device according to claim 56, wherein the control gate and the upper electrode are electrodes that are formed from metal.

10 65. A semiconductor device according to claim 56, wherein the control gate and the upper electrode are electrodes that are formed from salicide.

66. A semiconductor device according to claim 56, wherein
15 the floating gate and the lower electrode are films that are formed in the same step, and
the control gate and the upper electrode are films that are formed in the same step.

20 67. A semiconductor device according to claim 51 or claim 52, wherein the capacity element is a component of an analogue circuit.

68. A semiconductor device according to claim 51 or claim 52, wherein
the non-volatile memory transistor includes split-gate type non-volatile
25 memory transistor.

69. A method for manufacturing a semiconductor device having a structure that includes a non-volatile memory transistor and a capacitor element formed in one semiconductor substrate, wherein

the non-volatile memory transistor includes a floating gate, an intermediate insulation film and a control gate, and

the capacitor element includes a lower electrode, a dielectric film and an upper electrode, the method comprising the steps of:

- (a) forming the floating gate and the lower electrode on the semiconductor substrate;
- (b) forming a first oxide film on the floating gate and the lower electrode;
- (c) forming a second oxide film on the first oxide film;
- (d) forming a nitride film that becomes a component of the dielectric film on the second oxide film on the lower electrode;
- (e) forming a third oxide film that becomes a component of the intermediate insulation film and a component of the dielectric film on the second oxide film on the sidewall of the floating gate and on the nitride film on the lower electrode, respectively; and
- (f) forming, after the step (e), the control gate and the upper electrode on the semiconductor substrate.

70. A method for manufacturing a semiconductor device according to claim 69, wherein the step (a) includes the step of introducing an impurity in the lower electrode to provide the lower electrode with a predetermined impurity concentration.

71. A method for manufacturing a semiconductor device according to claim 69, wherein the first oxide film is formed by thermal oxidation.

72. A method for manufacturing a semiconductor device according to claim 69, wherein the second oxide film is formed by CVD.

5 73. A method for manufacturing a semiconductor device according to claim 72, wherein the CVD includes a high-temperature CVD.

74. A method for manufacturing a semiconductor device according to claim 69, wherein the nitride film is formed by CVD.

10 75. A method for manufacturing a semiconductor device according to claim 69, wherein the third oxide film is formed by thermal oxidation.

15 76. A method for manufacturing a semiconductor device according to claim 69, wherein the step (d) includes the steps of:

forming a nitride film on the second oxide film;

forming a mask film on the nitride film on the second oxide film on the second lower electrode; and

20 selectively removing the nitride film by an anisotropic etching, using the mask film as a mask, to leave the nitride film that becomes a component of the intermediate insulation film and a component of the dielectric film on the second oxide film on the sidewall lower section of the floating gate and on the second oxide film on the lower electrode, respectively.

25 77. A method for manufacturing a semiconductor device according to claim 69, wherein the step (a) includes the step of forming a selective oxide film on the floating gate.

78. A method for manufacturing a semiconductor device according to claim 77, wherein the step of forming the selective oxide film includes the steps of:

forming a conductive film on the semiconductor substrate; and

5 forming the selective oxide film on the conductive film that becomes the floating gate.

79. A method for manufacturing a semiconductor device according to claim 78, wherein the floating gate is patterned, using the selective oxide film
10 as a mask.

80. A method for manufacturing a semiconductor device according to claim 69, wherein the step (a) includes the step of:

forming a conductive film on the semiconductor substrate; and

15 patterning the conductive film to form the floating gate and the lower electrode at the same time.

81. A method for manufacturing a semiconductor device according to claim 69, wherein the step (f) includes the steps of:

20 forming another conductive film on the semiconductor substrate; and

patterning the another conductive film to form the control gate and the upper electrode at the same time.

82. A method for manufacturing a semiconductor device according to
25 claim 69, wherein the non-volatile memory transistor includes a split-gate type non-volatile memory transistor.